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Large-area two-dimensional silicon photonic crystals for infrared light fabricated with laser interference lithography

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Abstract
We report on the production of large-area 2D photonic crystals from high-index material with laser interference lithography (LIL). A new image reversal photoresist is used in combination with an anti-reflection coating to suppress undesired reflections. The photonic crystals possess a cubic pattern of air holes in a 500 nm silicon layer and cover an area of 1 cm^2.

1. Introduction

We demonstrate a novel process to fabricate two-dimensional (2D) photonic crystals from high-refractive-index materials, such as silicon on insulator, with laser interference lithography. During lithographic exposure Fresnel reflection and corresponding standing wave formation, normally leading to detrimental pattern deformation, is suppressed by including an additional anti-reflection coating. The fabrication process yields a LIL-patterned chromium mask that allows for higher etching depths in slowly etching substrates.

Two-dimensional (2D) photonic crystals (PhCs) [1] promise potential applications in integrated optical devices [2]. Such crystals can be realized from a slab waveguide, which consists of a thin film of high-index refractive material placed on a low-index substrate. Within the plane of the film the refractive index is periodically varied with a period of the order of the relevant wavelength. The resulting band structure for the guided modes in the plane of the slab allows a large degree of control over light propagation.

2. Experimental details

Conventional techniques to fabricate 2D PhCs with deliberately located light guiding defects are e-beam lithography (EBL) [3, 4], a focused ion beam (FIB) [5], and deep-UV lithography [6, 7]. The main drawback of EBL and a FIB is their sequential nature. As a result they are relatively slow and prone to drift, i.e. less useful for applications that require large areas of highly periodic lattices. Deep-UV lithography can be used to fabricate 2D PhCs on a large scale with arbitrary patterns in a single exposure step. However, the required lithography mask still has to be written with an e-beam. Furthermore, deep-UV lithography is costly, as it requires a deep-UV laser and a wafer stepper as well.

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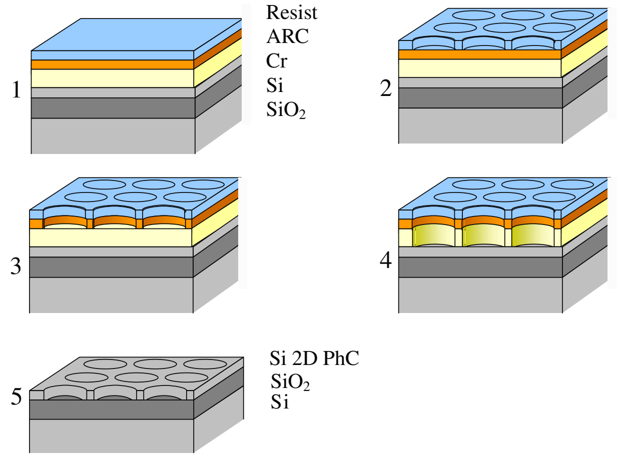

Figure 1. Sequence of the main experimental steps for the fabrication of 2D Si PhCs from an SOI wafer: a photoresist layer (0.9 μm) on top of an ARC (0.2 μm), Cr (0.2 μm), Si (0.5 μm), SiO_2 (3 μm), and a Si wafer (1) is patterned into a large-area hole structure with LIL and resist development (2); thereafter follows reactive ion etching into the ARC layer (3), wet etching into the Cr layer (4), and reactive ion etching into the Si top layer of the SOI wafer (5). The layer thicknesses shown are not to scale.

(This figure is in colour only in the electronic version)

In comparison to the latter methods, laser interference lithography (LIL) [8, 9] is a relatively simple technique to obtain large-area 2D PhCs with a well defined periodicity. Here, typically two beams with large (cm^2) cross-section from a standard UV laser are superimposed to form an interference pattern of well controlled periodicity on a substrate coated with photoresist. In addition LIL can be combined with a sequential writing technique, like a FIB, to place additional light guiding defects into a pre-made periodic structure [8].

Unfortunately LIL, as it has been applied so far, suffers from important drawbacks. First, if PhCs with high index contrast are to be fabricated (such as from Si or GaAs), the high Fresnel reflectivity of the substrate causes standing wave patterns in the resist that result in an unwanted vertical and usually detrimental modulation of the desired resist pattern. The successful application of LIL to high-index materials therefore requires the suppression of this standing wave pattern. Second, the etching depth into slowly etching substrates is limited, if the resist patterned by LIL is used as the etch mask itself. Rather, it would be desirable to first transfer the resist pattern into a stable mask (such as Cr) before etching into the substrate.

In this paper we describe a novel LIL fabrication process for large-area, high-index substrates that avoids the named disadvantages and thus enables its application to SOI (silicon-on-insulator) technology. It uses an additional antireflection coating (ARC) that suppresses standing-wave-induced pattern deformation in the resist. Furthermore, the fabrication process yields a LIL-patterned Cr mask allowing for high etching depths in the substrate. We demonstrate these advantages by fabricating highly periodic, high-contrast Si 2D PhCs with sizes in excess of 1 cm^2.

Figure 1 shows an overview of the fabrication steps involved. We begin with a commercially available SOI bulk wafer[7] with a 1.5 μm thickness of the silicon (Si) top layer. This high-index top layer ($n \approx 3.4$ @ $\lambda = 2.5$ μm) is monocrystalline and is separated from the 522 μm thick Si wafer by a 3 μm thick silicon oxide layer with low index ($n \approx 1.4$). As we aim at fundamental mode waveguiding at a wavelength of 2.5 μm, the first step is to reduce the thickness of the Si top layer to about 0.5 μm with chemical mechanical polishing and reactive ion etching (RIE). After this step the measured surface roughness is less than 3 nm (RMS) as checked by atomic force microscopy and scanning electron microscopy (SEM). Nitric acid and water combined with oxygen plasma etching are used to clean the surface. Next, a 25 nm thick Cr layer is deposited on the silicon top layer using an electron gun evaporation source. Then, an ARC layer is spin coated on top of the Cr layer. As the ARC layer we used Barli II[8], which contains a polymer doped with light absorbing dyes. An adjustment of the spin speed to 3000 rpm for 30 s and an adjustment of the viscosity by adding solvent is used to set the ARC layer thickness to 200 nm, as our calculations show that this thickness would result in a sufficiently low amplitude of the light reflected from the Cr layer (a reflection reduction by a factor of ∼10). A pre-bake step at 200 °C for 60 s is performed to drive off the remaining solvent. Finally, a 0.9 μm thick layer consisting of a prototype image-reversal resist is spin coated at 3000 rpm for 30 s. The resist (Clariant TI09 XR) (see footnote 8) contains a photoactive compound that responds to the entire UV spectrum from 310 to 440 nm due to additional chemical components, which bring about the image reversal.

To expose the resist with a periodic stripe pattern of light, two beams with an intensity of 90 $\mu W\ cm^{-2}$ each from a continuous-wave UV Ar ion laser (Spectra Physics, wavelength 363.8 nm) are superimposed at an angle. With an angle of 11° we obtain a highly accurate period of the pattern of 1 μm. The diameter of the beams is about 3 cm, as limited by the size of the optical components available to us, and the exposure time is typically 40 s. The result of a single exposure is a 1D line pattern. For the construction of a 2D pattern, a second exposure is necessary. In between these two exposures, the wafer sample is rotated around its surface normal by 90°, resulting in a square pattern. A rotation of 60° between two such exposures was used to obtain a triangular surface pattern.

After the LIL exposures, the wafer is heated to a temperature of 125 °C for 120 s. At this elevated temperature, the constituent of the photoresist that has received its threshold UV dose reacts with the added chemical component and becomes permanently insoluble in the developer. Then, the photoresist is flood exposed for 30 s using a UV lamp at an intensity of approximately 12 $mW\ cm^{-2}$, followed by development with AZ 400 K developer (see footnote 8) for 20 s. During the development, all photoresist that did not receive the threshold dose in the two LIL exposures, was removed. The resulting resist structure is shown in figure 2 as recorded with SEM. The structure covers an area of about 1 cm^2 and consists of a square array of holes with an excellent 1 μm periodicity (measured error less than 1%). The shape of the photoresist holes is round and uniform, with a size polydispersity of less than 6%.

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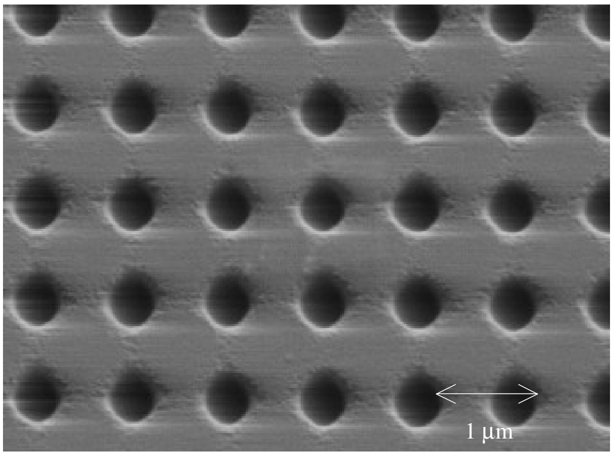

Figure 2. SEM micrograph of the structured image reversal photoresist. The high definition of the holes is clear. The measured periodicity is 1 μm.

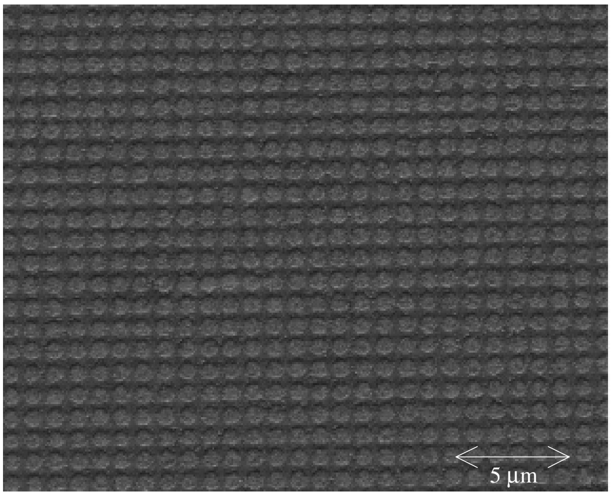

Figure 3. SEM micrograph of the hole structure transferred into the Cr layer.

After fabricating the hole structure in the resist, reactive ion etching (RIE) is performed for 2 min to deepen the hole pattern further into the ARC layer. Care is taken that RIE completely removes the ARC within the holes. The latter is checked via a local chemical element analysis of the surface with an SEM machine equipped with energy dispersive x-ray analysis. Thereafter Cr wet etching is performed to transfer the hole structure into the Cr layer, where the photoresist–ARC double layer acts as the mask. Figure 3 shows an SEM picture of a correspondingly patterned chromium mask on top of an SOI wafer. It can be seen that the shape of the holes remains round, but the diameter of the holes is increased by about 10% compared with the structure in the resist layer (figure 2). The increased diameter is caused by the isotropic nature of the wet etch. Finally, the pattern in the Cr layer is transferred into the Si top layer by etching for 10 min with an ion-etching recipe based on oxygen and CHF_3. The etch depth is adjusted to a value of 0.5 μm via the O_2 flow (5 sccm) and the CHF_3 flow (25 sccm). The residual chromium is removed with a wet-etch solution of $HClO_4$ (10 ml), $Ce(NH_4)_2(NO_3)_6$ (33 g), and H_2O (400 ml). Figure 4 shows an SEM picture of the resulting 2D PhC sample, as cut out from the exposed area with a diamond saw. The crystal shows a periodic hole structure in the 0.5 μm thick Si top layer. The depth of the holes is 0.5 μm, such that the holes do not reach into the underlying low-index silicon oxide support layer, as measured with SEM at a side surface after cutting the sample. The measured periodicity of the structure is about 1 μm with a polydispersity of the hole diameter of less than 6%.

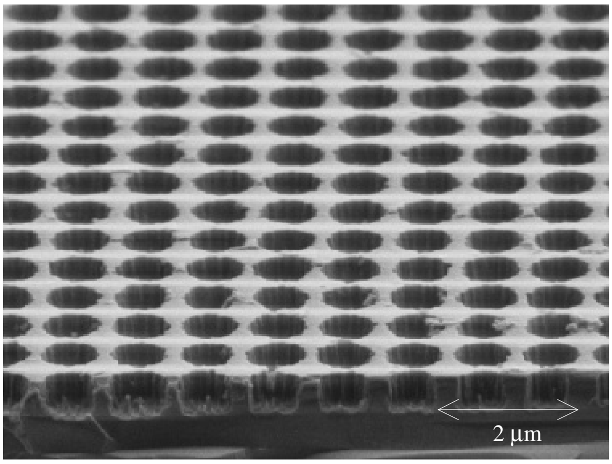

Figure 4. SEM micrograph of the cubic hole structure in the 0.5 μm thick Si top layer of the SOI wafer. The total area covered is about 1 cm^2. The holes are spaced by 1 μm and have a depth of 0.5 μm.

3. Conclusions

In summary, we have developed a new LIL fabrication process for large-area, highly periodic, 2D PhCs in high-index materials such as SOI wafers. The process involves a prototype image-reversal photoresist. An antireflection coating layer is used to suppress standing wave patterns in the resist. The resist pattern is transferred into a Cr layer to provide an appropriate mask for larger etching depths in the substrate. The process is demonstrated via the fabrication of silicon 2D PhCs. However, we expect that the process can easily be adapted for fabrication of 2D PhCs in other high-index materials, such as GaAs, or even metals.

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